REMARKS

In the Official Action mailed on **09 November 2009**, Examiner reviewed claims 1-2, 4-11, and 13-20. Examiner rejected claims 1, 10, and 19 under 35 U.S.C. § 103(a) based on Herlihy et al. (U.S. Patent No. 5,428,761, hereinafter "Herlihy"), and Hammond et al. (U.S. Patent No. 5,638,525, hereinafter "Hammond"). Examiner rejected claims 2, 4-7, 9, 11, 13-16, 18 and 20 under 35 U.S.C. § 103(a) based on Herlihy, Hammond, and Rajwar et al. (U.S. Patent No. 7,120,762, hereinafter "Rajwar"). Examiner rejected claims 8 and 17 under 35 U.S.C. § 103(a) based on Herlihy, Rajwar, and Hecht et al. (U.S. Pub. No. 2003/0064808, hereinafter "Hecht").

Rejections under 35 U.S.C. 103(a)

Examiner rejected claims 1, 10, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Herlihy, in view of Hammond. Applicant respectfully disagrees with the rejection. Herlihy and Hammond nowhere disclose, either separately or combined, that each entry in the store buffer includes a data value for a store operation that is to be committed to a memory address.

As discussed in Applicant's remarks filed on 29 July 2009, Herlihy discloses only: (1) an internal register set structure and (2) writing a value from a register to the cache and/or memory. Herlihy nowhere discloses committing store buffer entries generated during transactional execution to memory, wherein the store buffer is a separate structure in hardware from a register file.

Hammond discloses a processor that includes separate sets of registers. As is generally known in the art, a register can hold intermediate values, e.g., values for computations that may not be committed to memory. For example, processors generally include instructions to perform operations (e.g., add, subtract) using values in one or more registers. Some of these instructions can

store the result of the operation in a register, without ever committing the result to memory. In other words, a register can include a data value that is not committed to a memory address.

Applicant respectfully points out that the store buffer of the claimed embodiments is fundamentally distinct from a register, because each entry in the store buffer includes a data value that is to be committed to a memory address. More specifically, the claimed embodiments include a register file, and a separate store buffer. In embodiments described in the instant application, the system performs a store operation during transactional execution of a critical section.[1] The described embodiments store mark a cache line corresponding to the store.[2] After the cache line is store marked, these embodiments enter data for the store into an entry in the store buffer.[3] In other words, **entries in the store buffer are associated with a memory address because data values for these entries are associated with a cache line**. For example, as is generally known in the art, data in a cache line is read from and/or written to a main memory, i.e., the data is associated with a memory address. As described in the instant application, the data values for the store operation can be committed to memory if the transaction completes successfully. Herlihy and Hammond nowhere disclose, either separately or combined, that each entry in the store buffer includes a data value for a store operation that is to be committed to a memory address.

Accordingly, Applicant has amended the independent claims to clarify that each entry in the claimed store buffer includes a data value for a store operation that is to be committed to a memory address. These amendments find support in pars. [0072]-[0074], and FIG. 6 of the instant application. No new matter was added. Herlihy and Hammond nowhere disclose, either separately or

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1 see instant application, par. [0072]; also, FIG. 6
2 see *id.*, par. [0073]
3 see *id.*, par. [0074]

combined, that each entry in the store buffer includes a data value for a store operation that is to be committed to a memory address.

Hence, Applicant respectfully submits that independent claims 1, 10, and 19 as presently amended are in condition for allowance. Applicant also submits that the dependent claims that depend upon these independent claims are in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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